THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Quarterly Report #2

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by the

Center for Wireless Integrated MicroSystems
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

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Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this new contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/3B), the neural signals are buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals are amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past quarter, we have continued to explore ways to increase the single-unit recording lifetime of chronically-implanted probes. During the past quarter we have continued to follow an 8-shank probe implanted in guinea pig cortex with a large site at the tip (1000μm^2) and a smaller site in the center of the shank 25μm above it (177μm^2). These sites are still recording neural activity after 165 days and will be tracked until they are no longer viable. We are also continuing to explore biopolymer coatings for the probes to modify the tissue reaction to them. These materials can attract neural growth to the probe surface or can reduce adsorption of proteins there. We have deposited polypyrrole and polyethylene glycol on different probes and implanted them in guinea pig cortex. No adverse reaction to these biopolymers is seen three weeks post-implantation histologically nor do the coatings seem to affect the quality of the recordings obtained. More implants with these coatings will be implanted for longer periods of time to further study the tissue reaction to them.

Working with Foster-Miller, Inc., of Waltham, MA, we have developed liquid-crystal polymer-based ribbon cables for the chronic implantation of the probes. The capbles are 25μm and 50μm thick and from 2cm to 9cm in length. The leads are gold and nickel over copper with a 150μm pitch. We are beginning to explore the flexibility and use of theseprobes in-vivo but the addition of an upper layer of LCP for encapsulation is needed. The cables join with a surface-mount Omnetics NANO connector, with connections made to a silicon ribbon cable using standard ultrasonic wire bonding.

In order to use the front-end-selected 64-site 8-channel probe PIA-2B in-vivo, we have developed a Labview-based user interface for it that allows the user to select recording or test modes and any of the possible site configurations. This probe is now in use in Gyorgy Buzsaki's laboratory at Rutgers and experiments with it here at the University of Michigan are planned for the coming quarter.

In order to successfully fabricate the multiplexed probe, PIA-2, and its 3D counterpart, PIA-3, we have designed and simulated a series of amplifiers for potential use on the probes. These amplifiers offer a gain of 100, bandwidth from 10Hz to 10kHz, power dissipation of 150µW, input-referred noise of 6µVrms/rt.Hz, and a layout area of about 0.084mm^2. They are capacitively coupled to the electrode and differ in the techniques used for input dc bias stabilization. One design uses diodes at the input and output nodes of the feedback capacitor to set the bandwidth and dc bias. A second uses a diode clamp only at the input node, and a third uses a periodically-active clamp transistor pair there. A final configuration uses subthreshold (always on) transistor clamps at input and output nodes to quench the battery and optical currents. The first version is being used for the implementation of PIA-2/-3 as well as with a probe designed for wireless operation with platform-mounted telemetry.

Finally, work has gone forward with the development of telemetry circuits for use with active probes. The latest circuits obtained from a MOSIS fabrication run have been evaluated and work as intended. The voltage regulator produces an output voltage of 5V with a variation of less than 2mV over an input voltage range of 8V to 13V. The variation with load is about 4mV/mA. This is excellent performance. The ripple rejection is 46dB at 4MHz. The regulator consumes 80µA. A Delta-Sigma Modulator has also been developed for the telemetry circuits with an overall power dissipation of 200µW.

In order to reduce the power consumption of the front-end circuitry so that it can function correctly even with very limited received power, some of the circuit blocks have been redesigned and the on-chip power supply voltage has been decreased from 5V to 3.3V. The voltage regulator has been modified for this reduced supply voltage and a new operational amplifier has been designed for lower voltage and increased power-supply rejection. The bandgap reference was also redesigned for the lower supply voltage as were the clock-recovery circuit, the amplitude-shift-keyed demodulator, and the voltage limiter. The redesigned front-end circuitry has a total power dissipation of 240µW at 3.3V. A Manchester decoder for neural signal transmission was also developed. A complete telemetry interface for the active probes will be submitted for MOSIS fabrication this summer with the goal of operating a probe wirelessly by fall.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal-processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining mechanical lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by three to four orders of magnitude, and the probe requires only a few leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing has

been developed (PIA-2B) along with a high-end multiplexed probe that includes gain (PIA-2). These probes are now being refined and applied to in-vivo applications. Investigations are on-going to better understand site encapsulation, which limits the lifetime of chronic recording structures, and telemetry is being developed to allow the probes to be operated over a wireless link, eliminating the percutaneous connector.

During the past quarter, we have continued to study recording lifetime as a function of site size, placement, and various biocoatings. Active probes (PIA-2B) are now in use and in-vivo data is being gathered. A series of amplifiers has been designed for study of the dc input stabilization of the recorded signals. These will be fabricated this summer along with PIA-2/-3. Work has also gone forward on a completely wireless probe system with the design of a sigma-delta-based analog-to-digital converter. Work in these areas is discussed in the sections below.

2. Passive Probe Development

Chronic Animals:

In a continuing effort in conjunction with the Center for Neural Communication Technology (CNCT) to extend the period of time that we can record from chronically-implanted electrodes, we have looked at varying the recording site placement along the electrode shank. In the previous quarterly report we had implanted guinea pig auditory cortex with an 8-shank recording electrode with sites placed at the tip (1000μm^2) and 25μm above that (177μm^2), representing our version of a microwire electrode (Figure 1).

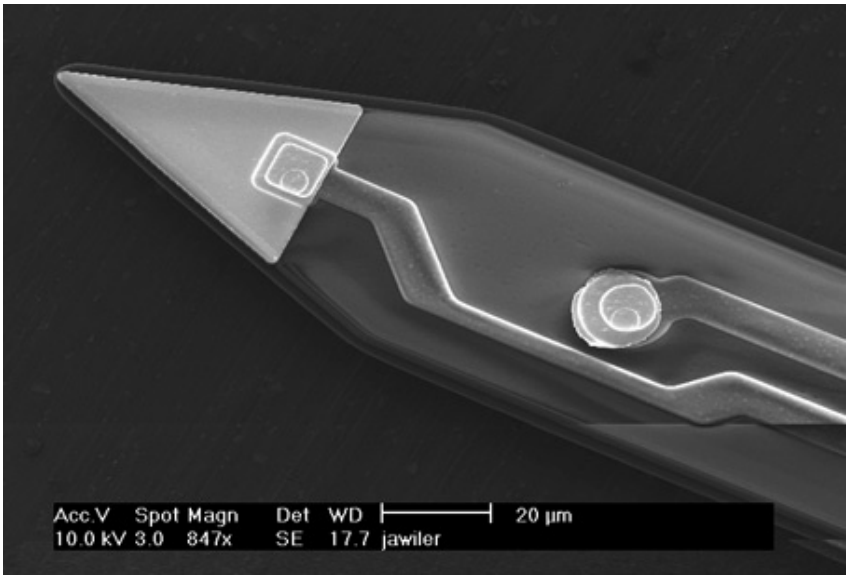

Fig. 1: SEM of a new probe designed to investigate the effects of tip site placement on chronic recording lifetime. In addition to a typical recording site in the middle of the shank, the probe has a site at the tip of the shank.

This electrode is still recording neural activity after 165 days (Fig. 2). Activity can be seen on both tip sites (odd numbered sites) and center sites (even numbered sites). Plots of the 1kHz impedances over time are shown in Fig. 3. Impedances have fluctuated for both site types but for the most part have stayed within the range of impedances that are capable of recording activity. We will continue to monitor this implant as long as it remains viable.

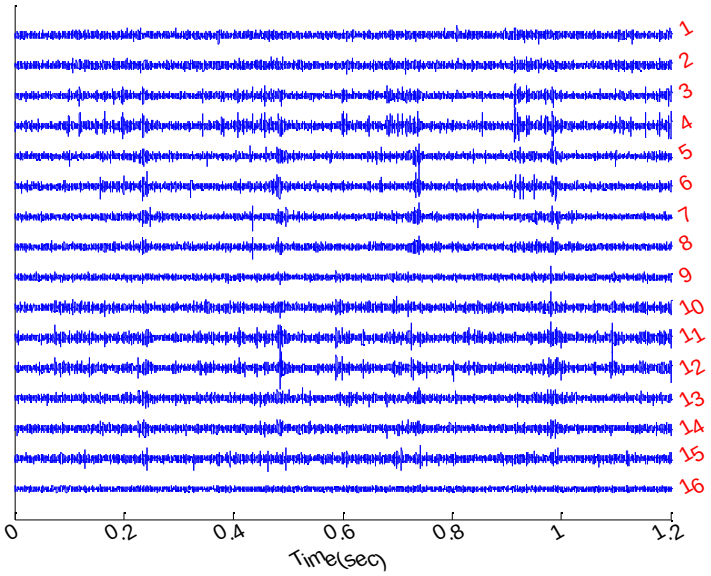

Fig. 2: Neural recordings taken 165 days post implant. Tip sites are odd numbered.

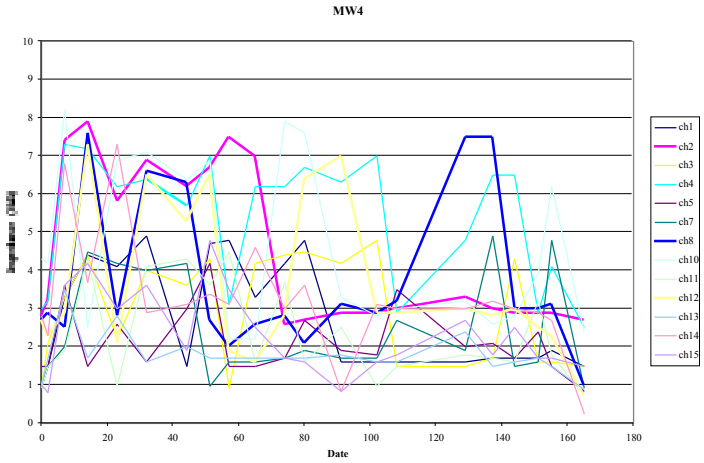

Fig. 3: Impedance data from a 16-channel electrode implanted in guinea pig auditory cortex. The tip sites are odd numbered.

Biopolymer Coatings:

In previous quarterly reports, we indicated that biopolymer coatings such as Polypyrrole and Polyethylene glycol (PEG) may help to improve the tissue reaction to the probes. Polypyrrole can carry agents to attract neural growth or restrict encapsulation. PEG is an agent that may reduce the adsorption of proteins on the metal surfaces thus keeping the impedance within an appropriate recording range (1-4MΩ). Working in conjunction with Professor David Martin and Xinyan Cui from the Materials Science and Engineering Department and the Macromolcular Center (for the polypyrrole) and Ms. Valerie Lee of the CNCT (for the PEG), we have deposited polypyrrole and PEG on separate electrodes and implanted them into guinea pig cortex. The first implants were not connected and were used for histological purposes only. Figures 4 and 5 show histology after 3 weeks of implantation. There is no adverse tissue reaction to these biopolymers beyond what is normally seen with an uncoated electrode.

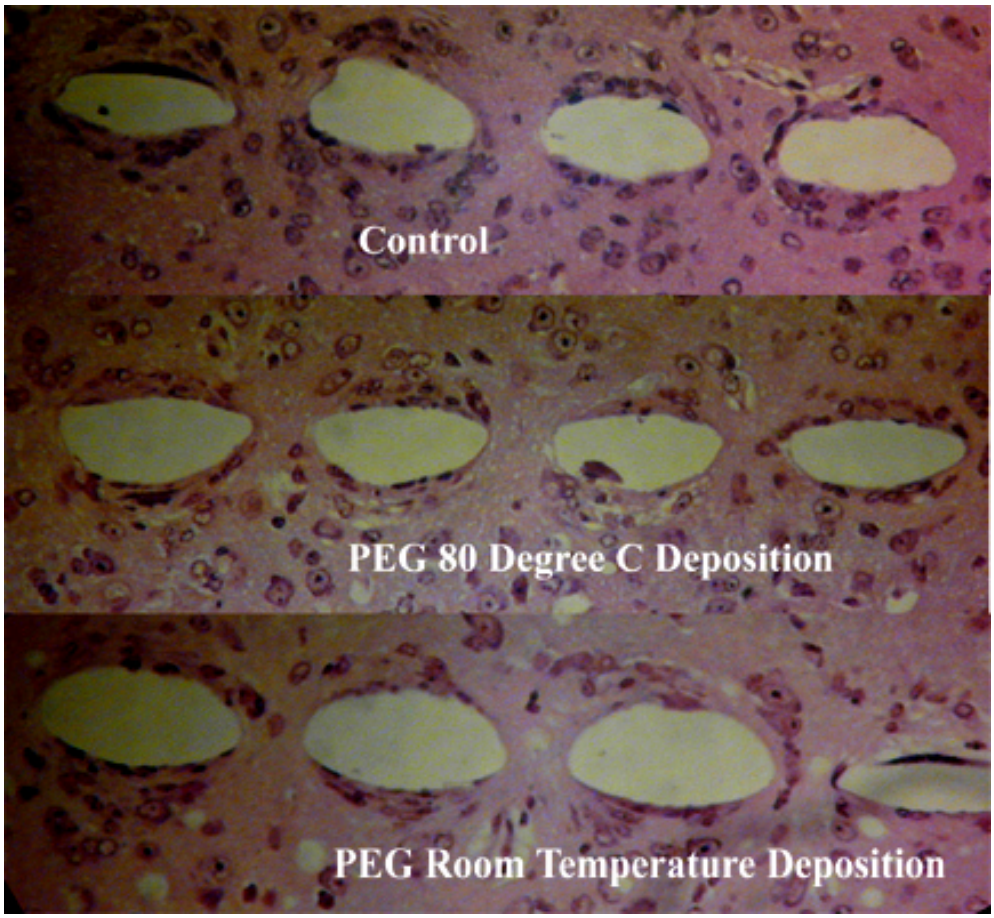

Fig. 4: Histological section through guinea pig cortex. There is no difference in tissue reaction between PEG-coated and normal silicon substrate electrodes.

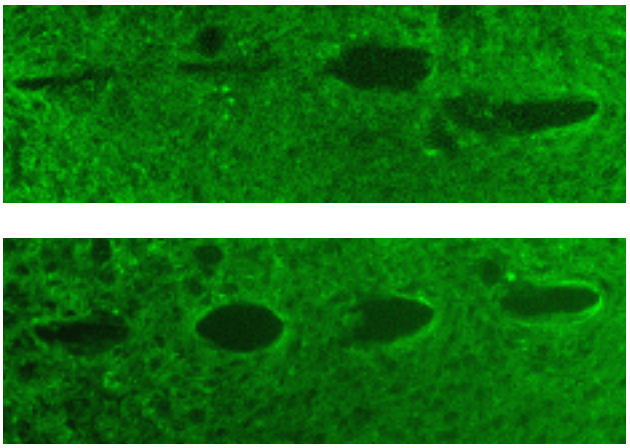

Fig. 5: Neurofilament staining of an electrode tract in guinea pig cortex. There is no difference in tissue reaction between normal silicon substrate electrodes (top panel) and polypyrrole coated electrodes (bottom panel).

We then implanted connected electrodes into guinea pig auditory cortex. Figure 6 shows neural responses after 2 weeks of implantation. We will continue to follow the PEG-implanted animal as long as it will record. The polypyrrole animal will be sacrificed at the end of 3 weeks and examined histologically

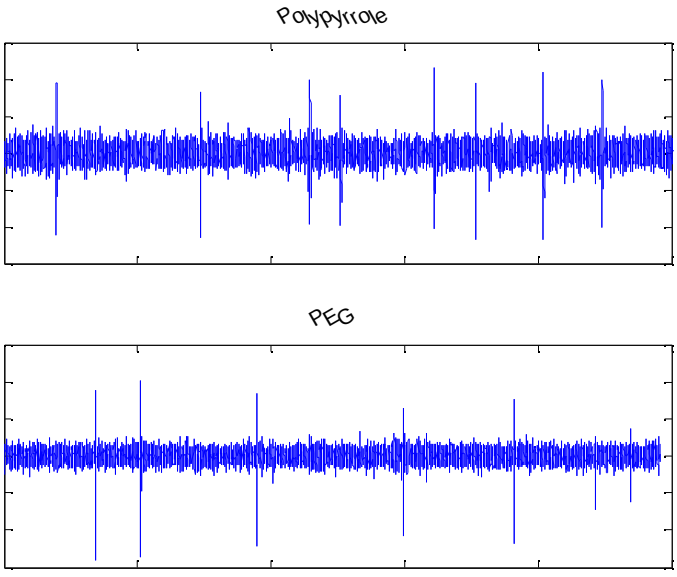

Fig. 6: Neural recordings from guinea pig auditory cortex for an electrode coated with polypyrrole (top panel) and another animal with an electrode coated with polyethylene glycol (bottom panel). The presence of the biopolymer coating has no effect on the quality of neural recordings obtained.

3. Packaging Developments

The statement of work for this contract requested that we develop or obtain a flexible microcable at least 8cm in length. In addition, it was stated that the 4mm of cable closest to the probe should be as flexible as a 100µm-diameter gold wire. We proposed to explore a hybrid system with an integrated silicon cable forming the first 4mm portion and a more robust cable forming the secondary portion of the interconnect.

One proposed type of secondary cable utilizes liquid crystal polymer (LCP) technology. We are working with Foster-Miller, Inc. of Waltham, MA, who has an NIH SBIR to develop LCP cables for this type of application. LCP has several features that make it an attractive cable candidate, including its flexibility and low moisture absorption. In addition, preliminary biocompatibility tests conducted for Foster-Miller are very encouraging.

Presently, Foster-Miller fabricates an LCP-based multilayer interconnect that is being used to realize all-plastic near-hermetic packages for microwave and digital receiver applications (Noll1, Noll2, Jayaraj). LCP films can be laminated with thin-film conductor foils by applying heat and pressure in a lamination press without the use of adhesives. The metal film can then be patterned using low cost flexible circuit manufacturing processes.

We received the first prototype LCP cables from Foster-Miller last month. Figure 7 shows a 16-channel chronic probe bonded to an LCP cable. The LCP device is designed to mate to an 18 pin surface-mount Omnectics NANO connector as shown. Both 1 mil- and 2 mil-thick LCP cables have been fabricated with total lengths (including connector region) ranging from 2 to 9cm. The leads consist of thin layers of gold and nickel over copper foil. The pitch on these particular cables is 6 mils so that they match the pitch of the standard probe bond pads.

These prototype LCP devices have no upper layer to passivate the leads. It may be possible for Foster-Miller to apply an upper LCP film although this technology is not yet fully developed. There are also other options, including thin epoxy coating of the leads. We will explore these options in the coming months.

References:

[Jayaraj] K. Jayaraj, T. E. Noll and D. R. Singh, "A low cost multichip packaging technology for monolithic microwave integrated circuits," *IEEE Trans. on Antennas and Propagation*, 43(9), Sept. 1995.

[Noll1] T. E. Noll, K. Jayaraj, B. Farrell, T. Perkins and D. Glynn, "A low cost phased array antenna packaging technology," *1996 Antenna Applications Symposium*, Allerton Park, IL, Sept. 1996.

[Noll2] T. E. Noll, K. Jayaraj and B. Farrell, "A low-cost near hermetic multichip module based on liquid crystal polymer dielectrics," Fourth Issue of 1996 *International Journal of Microcircuits and Electronic Packaging*, 1996.

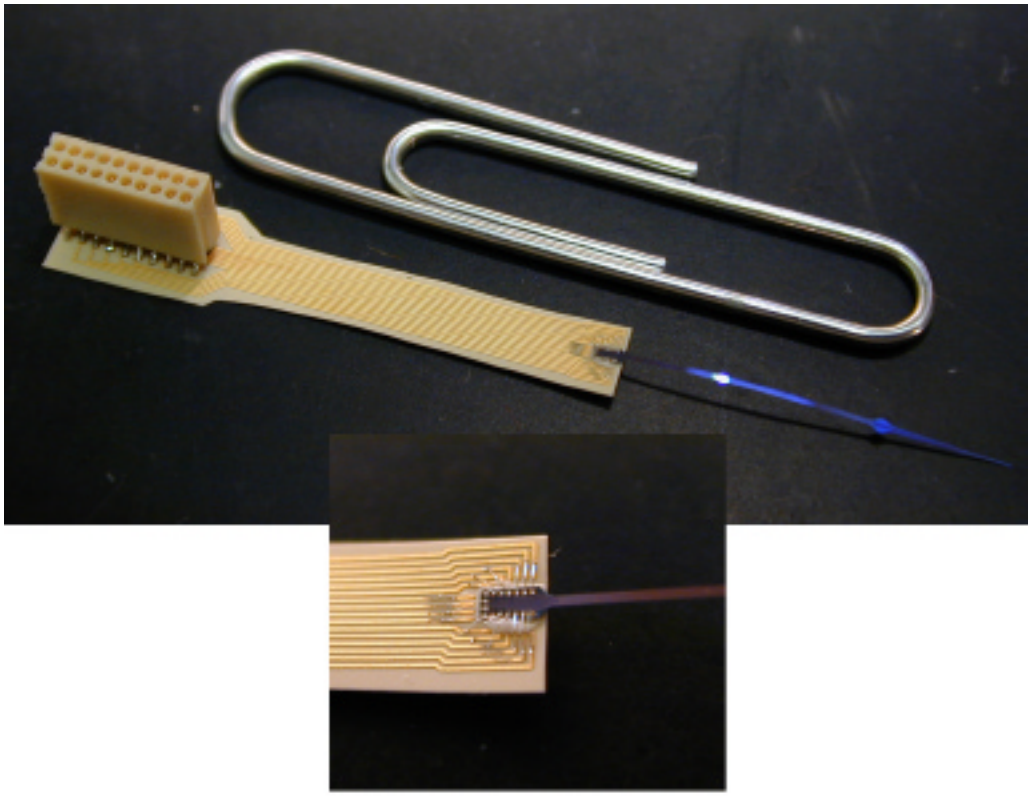

Fig. 7: Hybrid chronic assembly constructed from an integrated silicon cable/probe, an intermediate LCP cable, and a surface-mount Omnetics NANO connector. The total length of this structure, shown beside a standard paper clip, is 4cm from the tip of the probe to the back edge of the connector. Electrical connection between the silicon and LCP devices was accomplished using ultrasonic bonding.

4. Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)

During the past quarter, work has progressed on the testing of the 64-site front-end-selected and buffered probe "PIA-2B." The design and architecture of this probe have already been reported, and all digital and analog circuit blocks on the probe function as designed. In the last quarterly report, data were presented which demonstrated the ability of the probes to record spikes in-vivo. In these experiments, a probe with a simpler version of the digital control circuitry was utilized. This probe differed from PIA-2B only in the size of the digital data registers (3 bits instead of 24 bits) and hence in the number of allowed site selections. This simplification allowed easier utilization of the probes in an in-vivo setting. Sample results from these experiments are given in Fig. 8 and have already been described.

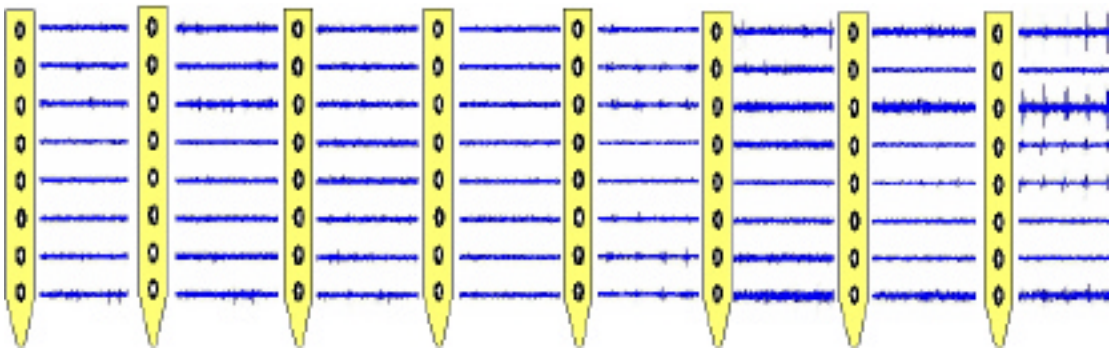

Fig. 8: Driven spikes in auditory cortex recorded with a front-end-selected probe. A sample sweep of all 64 sites reveals large, driven spikes only on shank 8.

In order to utilize the more flexible front-end-selected probe PIA-2B, work has been completed on the development of an interface system. This interface was written in Labview running on a pentium-based PC and allows the user to select probe recording and test modes and to select all possible site selection patterns. The interface system utilizes a National Instruments AT-MIO-16D data acquisition board. A screen capture of the control panel of the interface system is given in Fig. 9. At this point, the user enters a bit pattern to make mode and site selections --- knowledge of the site-selection wiring is necessary in order to use the system. The top level in the hierarchy of the wiring diagram for the interface is given in Fig. 10 along with a scope trace (Fig. 11) showing the output digital data corresponding to the selected front-panel data given in Fig. 9 (the serial bit stream is correctly reversed, with the most significant digit appearing last.)

Currently, PIA-2B is being tested in Gyorgy Buzsaki's laboratory at Rutgers University, with the hope of utilizing it in an experiment already in progress there. In the coming quarter, a graphical interface will be added to the control system to make site selection possible without entering bitstreams, and the whole system will be ported over to Buzsaki's laboratory. In-vitro and in-vivo experiments in guinea pig auditory cortex are also planned at the University of Michigan in the coming quarter. These experiments are being designed to illustrate the features of the PIA-2B probe.

In order to simplify testing of PIA-2B, an electrode jig was created (Fig. 12.) Currently, to test a probe, different site configurations are selected, and then the sites are probed under a microscope with a probe tip. The electrode jig has two perpendicular sets of large (brass) electrodes. After filling the jig with saline and inserting a probe, a large AC signal is input to a pair of electrodes. Using the linear voltage gradient thus created across the jig, it is possible to determine which site is selected, first along one axis, and then (by switching electrodes) along a perpendicular axis.

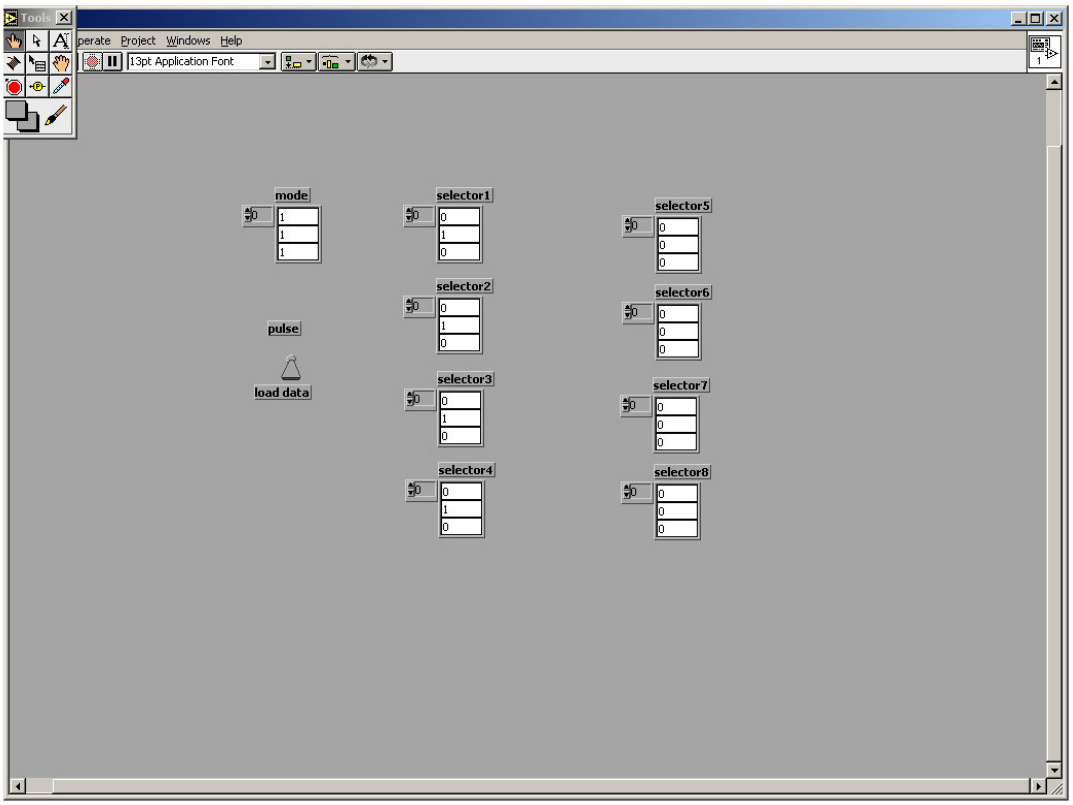

Fig. 9: Control panel of the PIA-2B probe. The toggle switches between loading the mode and selection data, and a pulse mode where the probe is interrogated for an "I'm okay" pulse.

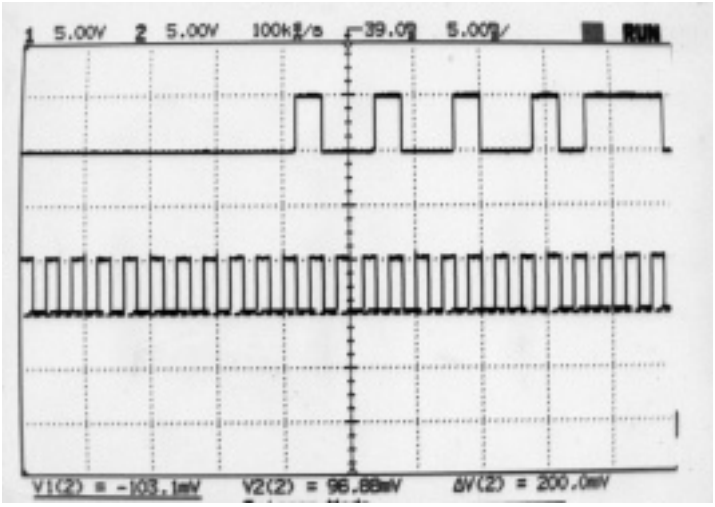

Fig. 11: Scope trace showing digital data output corresponding to bit stream selected in the control panel, above. The top trace is the first 25 bits of data (MSB last), and the bottom is the clock.

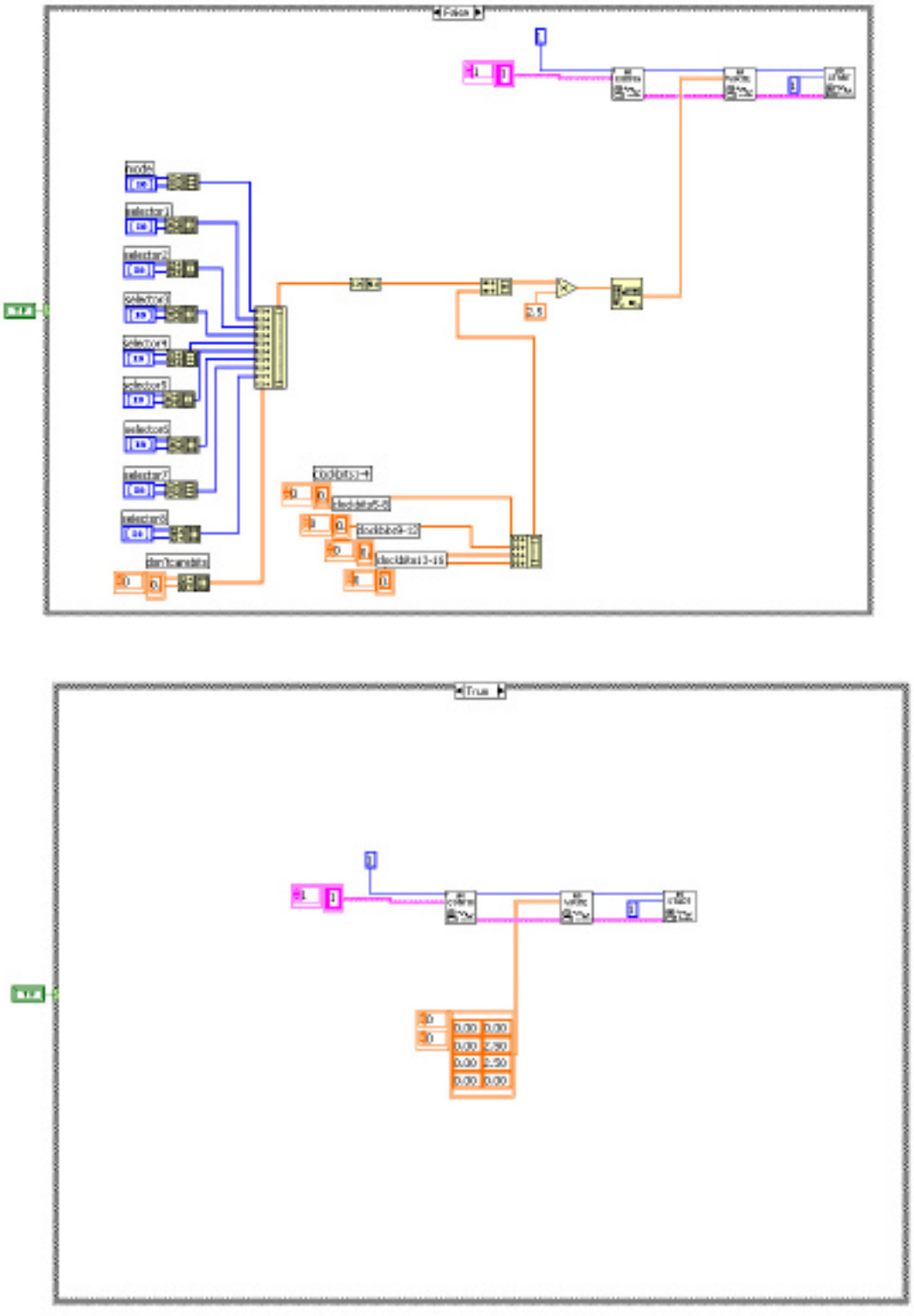

Fig. 10: Top level of the wiring diagram for PIA-2B interface.

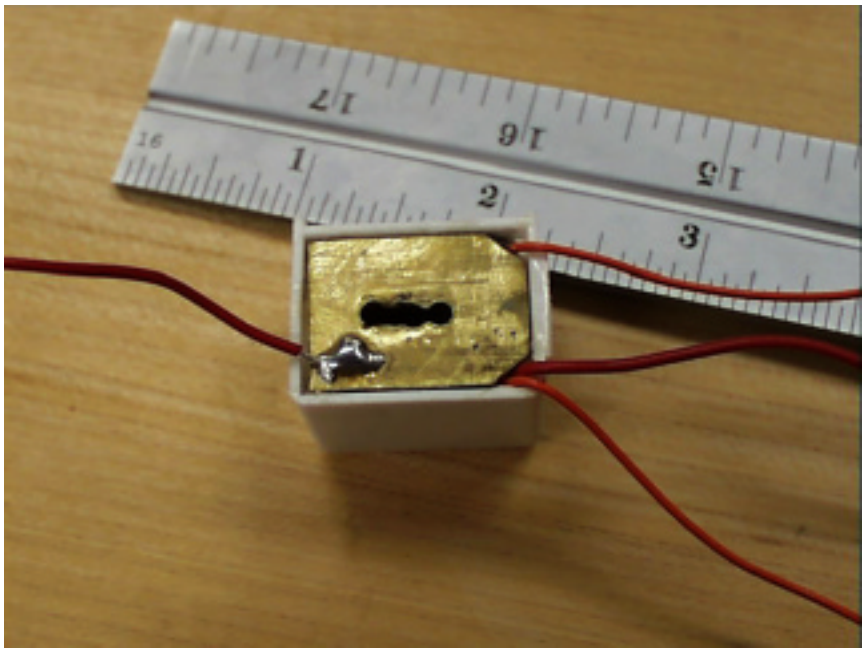

Fig. 12: Testing jig developed for testing active recording probes.

5. Readout Circuitry for Active Recording Probes

In preparation for the upcoming active probe fabrication run, four amplifier structures have been designed, layed out, and thoroughly simulated. The specifications of these amplifiers are quite similar and are summarized in Table 1. The first of these designs is pictured in Fig. 13. This feedback configuration was implemented on the previous process run and was successfully tested as reported in January of 2001. In an attempt to reduce the optical sensitivity of the structure, feedback transistors M1 and M2 have been placed in a grounded rather than floating P-well. This ac grounds the terminals of a large parasitic diode that was primarily responsible for the optical sensitivity problems encountered with the previous design. In addition, layout techniques such as gold and aluminum shielding have been used to reduce the amount of light that reaches MOS structures M1 and M2. Furthermore, these MOS structures have been placed in the center of the layout to reduce the amount of undercutting, i.e., backside illumination, they experience. The previous amplifier was designed assuming NMOS and PMOS threshold voltages of ±0.9V. The fabricated PMOS threshold voltage was measured to be –0.6V. While the measured amplifier performance matched well with the simulated values, proving the robustness of the design, some changes were made to increase the output swing. The amplifier configuration shown in Fig. 14 also uses a diode to achieve the high impedance necessary to eliminate the dc polarization of the electrode. This design incorporates all of the techniques listed above to reduce the sensitivity of the diode to illumination. There is no dc feedback path between the input and output nodes of the amplifier in this configuration, and this will lead to larger offset voltages at the output. The configuration presented in Fig. 13 is therefor preferable if both are optically insensitive.

Gain	40dB
Bandwidth	10Hz-10kHz
Power Consumption	150µW
Input Referred Noise	6µVrms/√Hz
Layout Area	0.084mm^2

Table 1: Approximate amplifier specifications

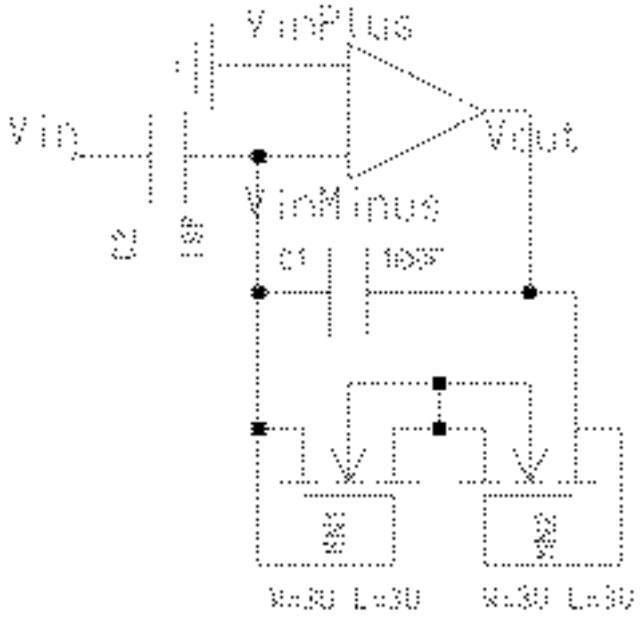

Fig. 13: Diode-connected feedback configuration used for an on-chip probe amplifier.

Two dc baseline stabilization techniques not based on diode impedances have also been implemented. Figure 15 pictures a reset gate that is used to filter the dc baseline potential of the electrode. The reset gate effectively switches capacitor C_2 to form an impedance given by

$$R_{eff} = \frac{1}{AC_2 f}$$

where A is the open-loop gain of the amplifier and f is the switching frequency. The reset frequency required to filter the dc baseline potential is on the order of 10Hz. The design pictured in Fig. 16 uses sub-threshold-biased transistors to attenuate the dc polarization of the electrode. The gates of the subthreshold transistors are controlled by the output of the op-amp. This negative feedback allows the design to be self-biasing. This is a vast improvement over previous subthreshold transistor designs, which had to be individually biased by an externally-controllable current source.

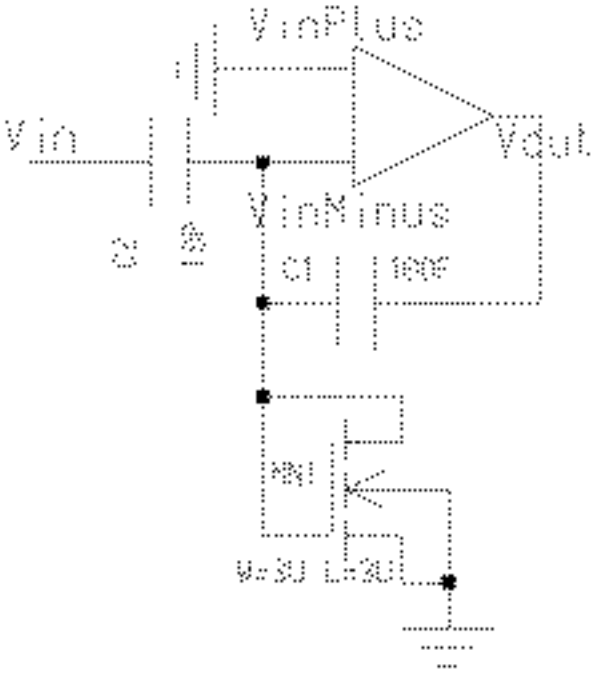

Fig. 14: Diode clamp circuit used in conjunction with a capacitively-coupled probe amplifier.

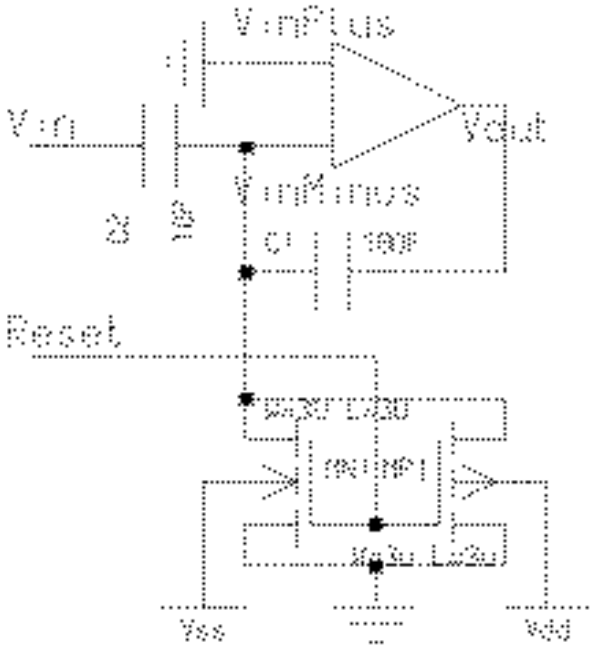

Fig. 15: Reset gate circuit used to set the dc input voltage of a recording electrode.

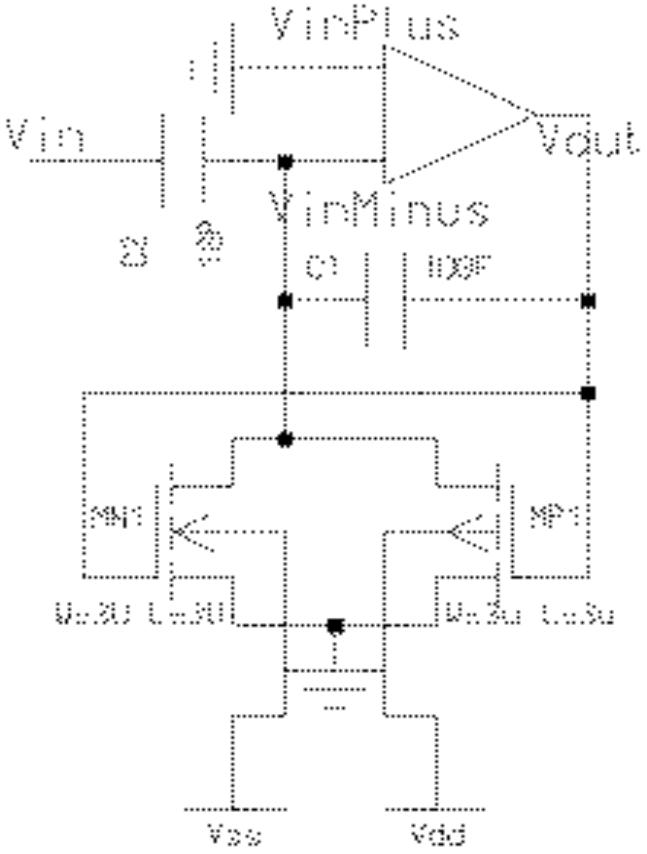

Fig. 16: Use of sub-threshold-biased transistors to stabilize the amplifier input voltage.

A 64 site, front-end selected, amplified, time-division-multiplexed neural recording probe will be included on the upcoming fabrication run. The probe will feature 64 sites that will be front-end selected down to eight sites for amplification. The amplifier shown in Fig. 13 will be used on this probe. Following amplification, the neural signals will be time-division-multiplexed onto one line. A previously fabricated and tested time-division-multiplexer design will be used (see quarterly reports July 2000 and Jan. 2001 for circuit and testing details). An active probe suitable for interfacing with a telemetric link will also be included on the upcoming run. The interface will be for one site only and will be amplified through the configuration shown in Fig. 13. An additional gain stage and single-ended-to-differential converter is currently being designed such that the entire dynamic input range of the platform-mounted A/D converter can be utilized.

6. Design of a Wireless Telemetry Platform for Multichannel Microprobes

Efforts on the design and testing of a wireless recording microsystem for multi-channel neural recording microprobes continued during the last quarter. Several tasks were completed in the last few months, including:

- Tested the chip submitted for fabrication in December 2000
- Completed layout and verified design of the delta-sigma modulator
- Improved the front-end circuitry to reduce power consumption
- Designed the Manchester decoder

6.1 Testing of the Fabricated Chip

The chip submitted last December, shown in Fig. 17, came back and the testing results match our expectations. The testing results of the bandgap voltage reference, clock regenerator were shown in previous reports. These circuit blocks are also used in this chip. All four chips received work well and show good consistency in terms of circuit performance specifications.

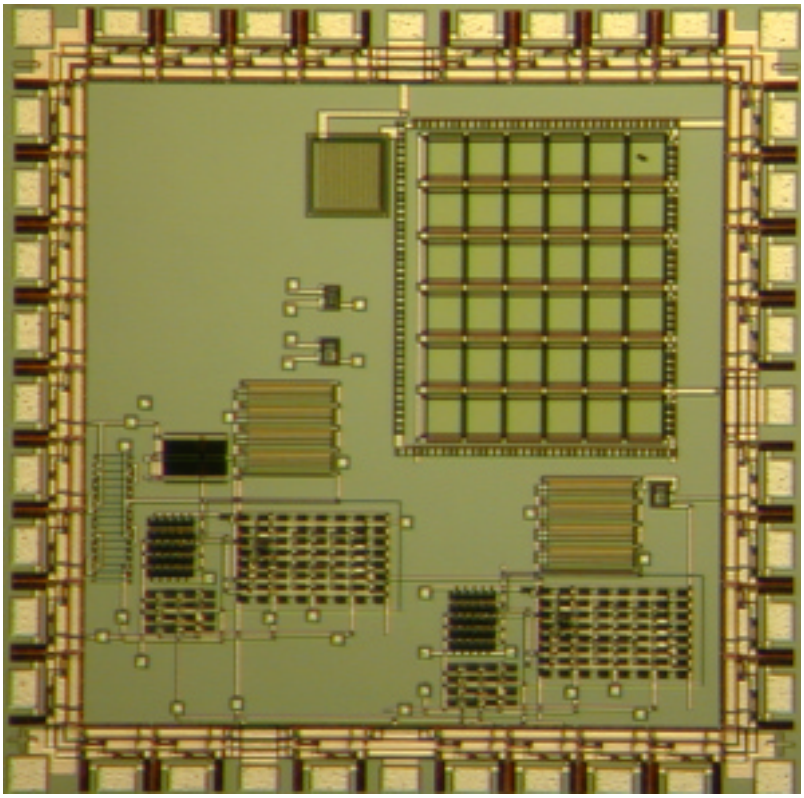

Fig. 17: Photograph of the test chip containing several of the front-end circuit blocks.

Figure 18 shows the output of the voltage regulator. As evident, voltage variation is less than 2mV/V when input voltage swings from 8V to 13V. The load regulation is shown in Fig. 19 and is about 4mV/mA.

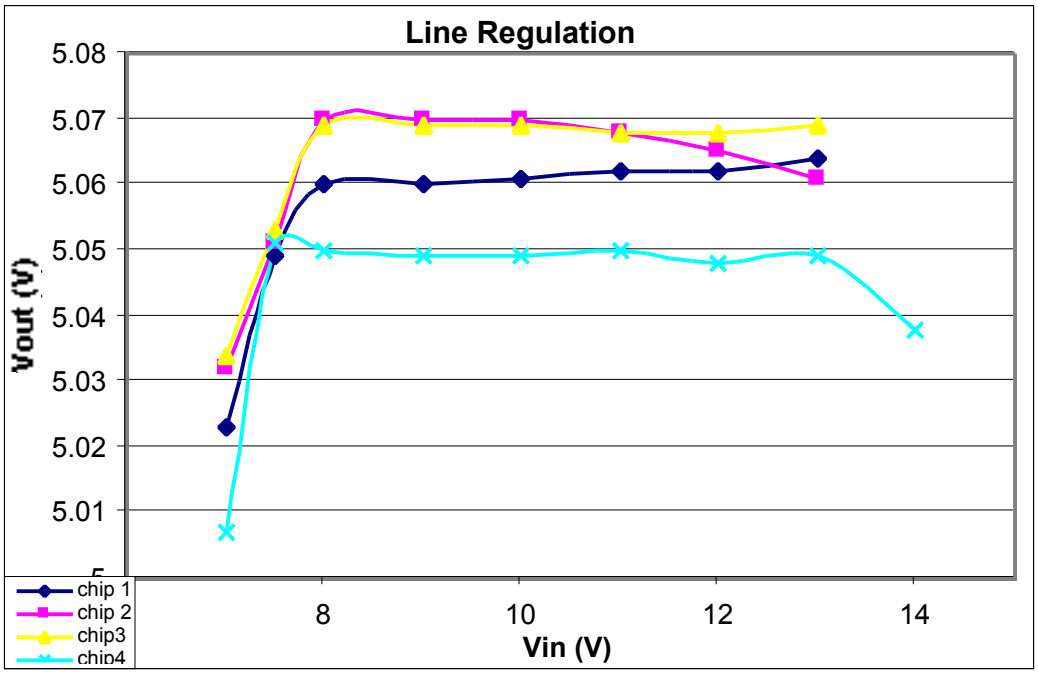

Fig. 18: Output voltage of the voltage regulator as a function of input voltage variation.

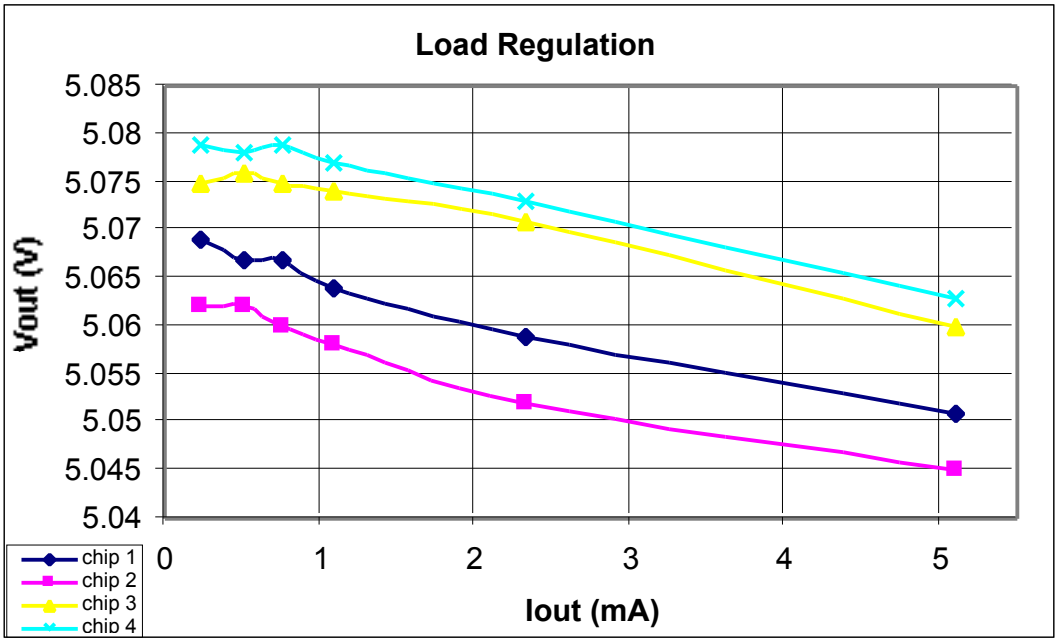

Fig. 19: Output voltage of the voltage regulator as a function of load current variation.

The ripple rejection ratio of the regulator is 46dB at 4MHz, which can be seen from Fig. 20. The input ripple of the regulator is 2V(p-p) and the output ripple is 10mV(p-p). This regulator shows very good ripple rejection characteristics at high frequency.

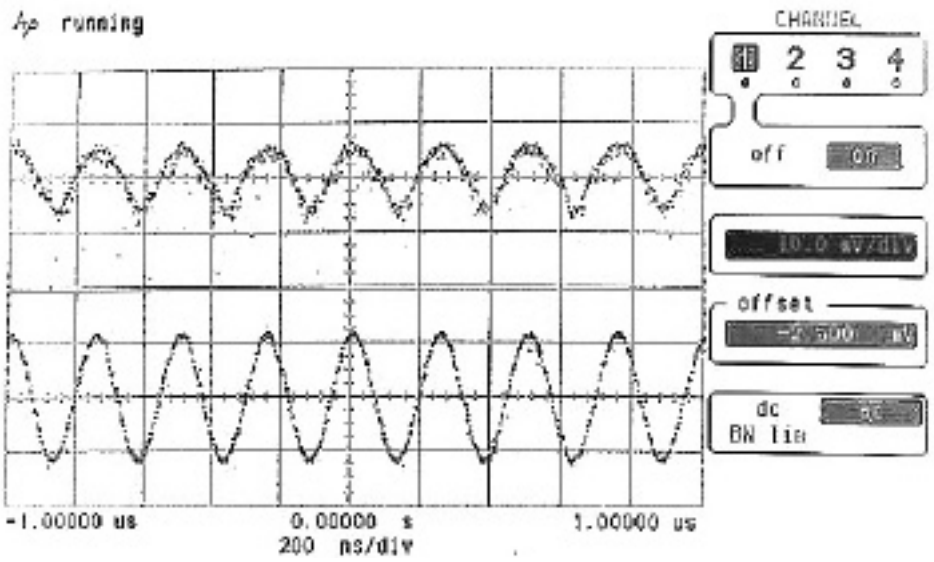

Fig. 20: Ripple rejection of voltage regulator.

The current consumed by the whole regulator, including bandgap reference, is 80µA in this design. The power consumption is also dependent on the input voltage of the regulator. An integrator in the sigma-delta modulator uses the same op-amp topology as the regulator, and it functions well.

6.2. Layout and Verification of the Sigma-Delta Modulator

The system and circuit schematic of a second-order sigma-delta modulator were shown in last quarterly report. The netlists were extracted from the layout and intensive simulation was carried on the sigma-delta modulator. The following plots show the simulation results.

Figure 21 shows the simulation waveforms when the input of Delta-Sigma Modulator (DSM) is a zero. The dif2 and dif1 are the outputs of the second-stage integrator and the first-stage integrator, respectively. We can see that the digital output is a square wave whose frequency is equal to half of clock frequency used by the DSM. This is as expected because the average of the output bits is obviously constant.

Figure 22 compares the reconstructed waveform with the original sinusoid input to DSM. DFT is also applied to the truncated input and reconstructed waveforms to compare their spectrum, shown in Fig. 23. The input and reconstructed waveforms and spectra match each other quite well.

Fig. 21: Delta-Sigma Modulator (DSM) simulation results when the input is zero.

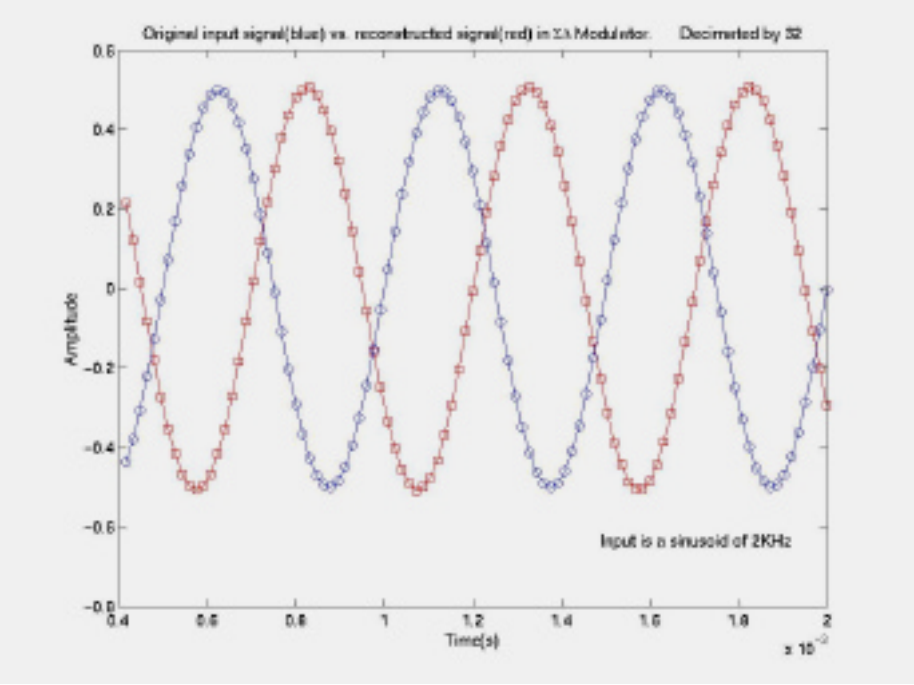

Fig. 22: DSM reconstructed waveform vs. the original input waveform.

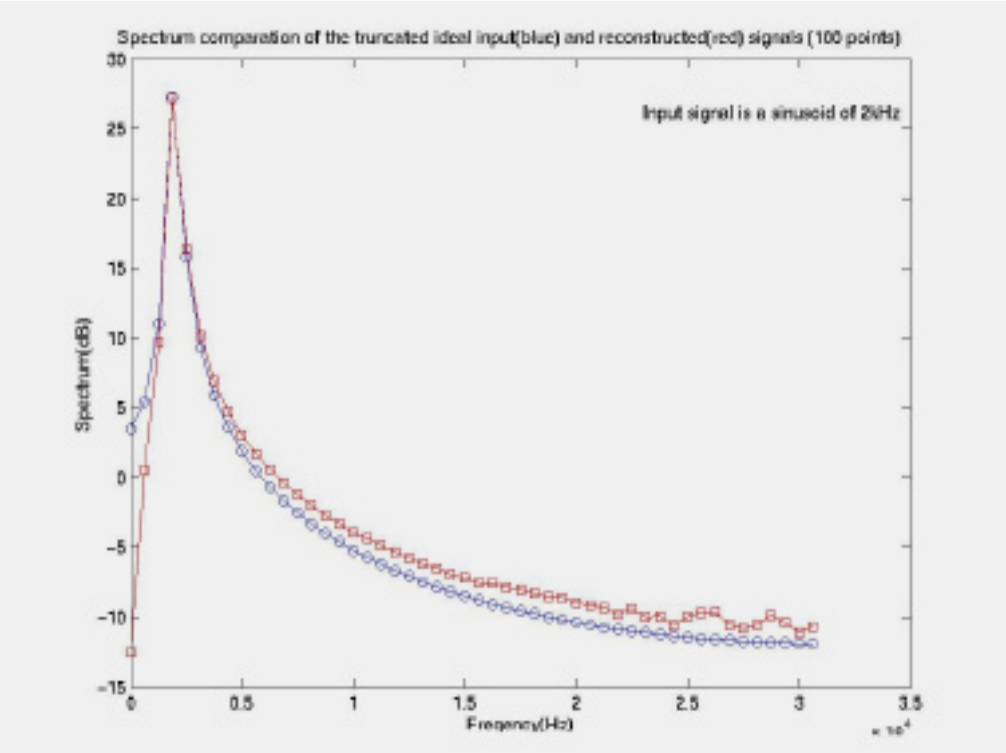

Fig. 23: Comparison of the spectra of input and reconstructed signals.

The bias current of the opamp used in DSM was reduced in order to minimize the power consumption, but still ensure that the opamp settling time satisfies the speed requirement of the DSM. The power consumption of the circuit blocks in DSM is listed in Table 2.

Table. 2: The power consumption of the DSM

Circuitry	**Power consumption Vdd=3.3V**
Two Integrators in DSM	2 x 50µW
Clock generator for DSM	70µW
1 bit ADC + CMFB	8µW (working at 2MHz)
Total power consumption for DSM	200µW

6.3. Improvement of the Front-End Circuitry

In order to reduce the power consumption of the front-end circuitry so that it can function correctly, even with very limited received power, some circuit blocks were redesigned and on-chip power supply voltage was decreased from 5V to 3.3V. We will show circuit schematic and simulation results in following sections. The bias currents in the new designs are set as low as possible, provided that the speed and settling time requirement are met.

Voltage Regulator

A series regulator is designed to provide power supply of 3.3V to on-chip electronics, as illustrated in Fig. 24. The receiver coil, D1 and C1 form a half-wave rectifier. The op-amp adjusts the current through the pass device Mpass according to the difference between the stable bandgap voltage reference and the negative feedback from Rf1 and Rf2. Consequently, Vdd is kept constant.

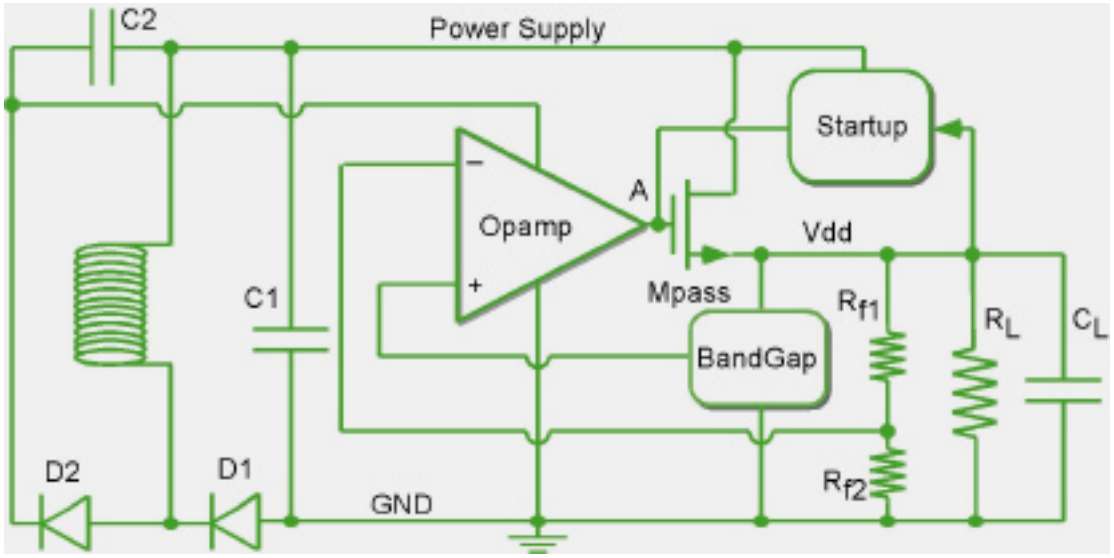

Fig. 24: Schematic of the regulator.

A npn BJT transistor can replace NMOS as the pass device but standard foundry CMOS processing does not provide NPN transistors. A PMOS can also be used as the pass device and achieve low dropout, however, the common-emitter configuration may lead to instability problem when load capacitance C_L changes in a wide range.

In order to solve the high dropout problem associated with NMOS pass device, a simple voltage-doubling block, made up of C2 and D2, is used to provide higher supply voltage to the opamp. As a result, the gate voltage of Mpass can be twice of the drain voltage of Mpass. The regulator begins to work correctly as long as the drain voltage of Mpass slightly exceeds the nominal voltage Vdd.

Note that the power supply of the bandgap reference is from the output of the regulator rather than the output of the half-wave rectifier; this configuration can lead to more accurate and stable voltage reference. On the other hand, this configuration needs a startup circuit; otherwise the regulator output and bandgap reference can always stay at zero.

In the design of the opamp, high PSRR is desirable because this can improve ripple rejection of the regulator. We will discuss the design of the bandgap reference and the opamp in following paragraphs.

A High PSRR Opamp

A high PSRR opamp is highly desirable in the regulator to reduce the high frequency ripple. The symmetric structure of the opamp, shown in Fig. 25, is helpful to cancel out the influence of the power supply ripple on the opamp output. Transistors M1, M2 and M3 form folded input stage, so positive common mode input range is increased. A cascode output stage is designed to obtain high gain. In addition, this is a one-stage opamp and has only one high-impedance point, so it is inherently stable when used in the negative feedback loop.

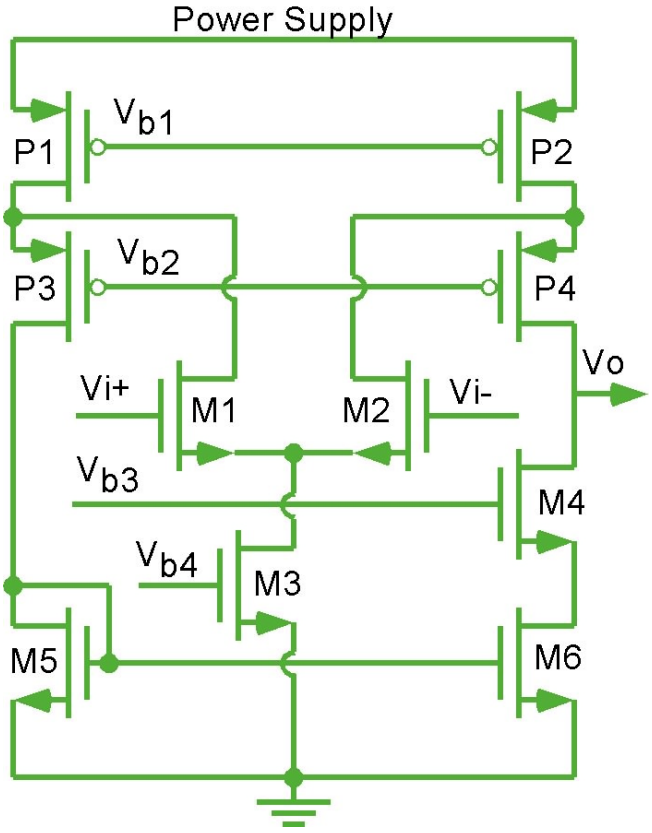

Fig. 25: Circuit diagram of the opamp used in the voltage regulator

Bandgap Voltage Reference

The bandgap reference provides accurate voltage reference for the regulator, and it is also used as current bias reference for other analog circuits. Because the power supply voltage is reduced to 3.3V, the cascode structure used before is not suitable any more. The new design is shown in Fig. 26. It can be shown that:

$$V_{BG} = V_{BE_2} + V_T \frac{R_2}{R_1} \ln(2M)$$

$$I_o = \frac{V_T}{R_1} \ln(2M)$$

If we set $I_o = 2\mu A, M = 3$

then $R_1 = 24k, R_2 = 312k$

The sizes of the transistors P1, P2, P3, M1 and M2 are designed to be big in order to obtain good matching and small channel length modulation. A shunt capacitor C between the output V_{BG} and Ground is used to improve PSRR at high frequency. Additional startup circuitry is necessary for the bandgap voltage reference to work in the desired point, which is not shown here.

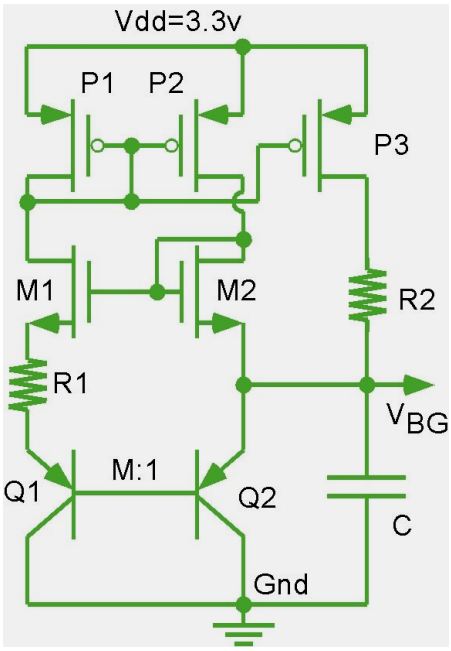

Fig. 26: Circuit diagram for the bandgap voltage reference.

Another simple regulator is designed to provide a power supply of 1.65V from 3.3V, which is supplied to the preamplifier on the active probe and the sigma-delta modulator. The schematic of this simple regulator is similar to that of 3.3V, which shares the same bandgap reference. The details of this circuit are not provided here.

The simulation result of the regulator is shown in Fig. 27. This simulation is based on the netlist extracted from the layout, so all the parasitic capacitances are taken into account. We can see that when the induced voltage across the receiver coil varies from 12V to 18V (peak-peak), the output voltages of the regulators stays at 3.3V and 1.65V, respectively. The bandgap reference also provides a stable reference voltage of 1.27V and bias current of 2µA.

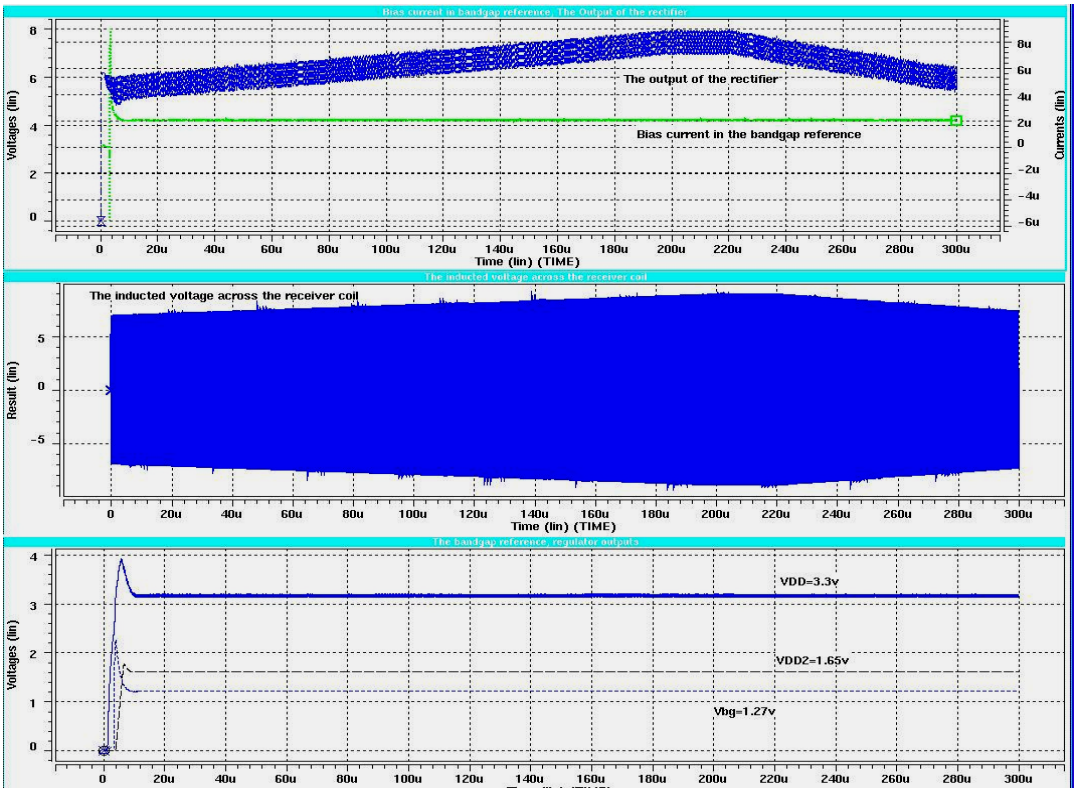

Fig. 27: Simulation results for the redesigned voltage regulator.

Clock recovery circuitry

The schematic of the clock recovery circuitry is shown in Fig. 28. Capacitors C01 and C02 form a voltage divider. Transistor NMOS P0 with a long channel length is used as a resistor. When the coil receives the sinusoid RF signal, the waveform at the gate of M2 is a sinusoid with an average of 1.65V. This waveform is compared with the constant voltage of 1.65V. Note that the second stage of the comparator uses a latch-type

differential stage. Transistors M3 and M4 switch the current sources so that current only flows during transition phases. The simulation result is shown in Fig. 29.

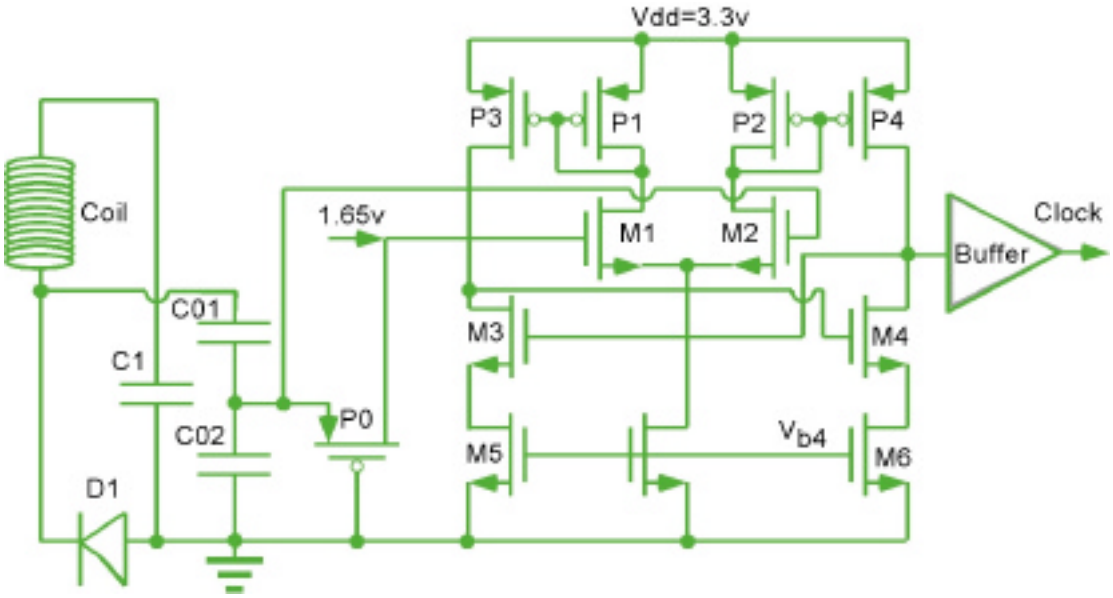

Fig. 28: The schematic of the clock recovery circuitry.

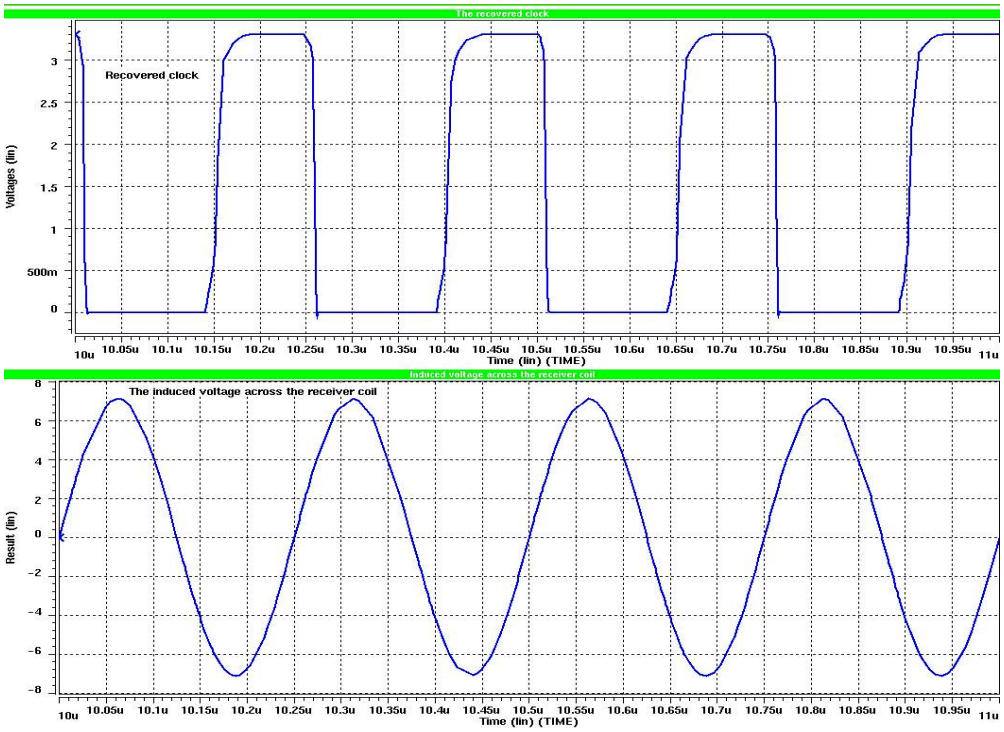

Fig. 29: Simulation results for the clock-recovery circuitry.

ASK Demodulator

Amplitude Shift Keying (ASK) will be used for data transmission. The ASK demodulator is designed to decode the commands from the modulated RF signal. Figure 30 shows the schematic of the ASK demodulator. Transistor P01 and capacitor C1 form a low-pass filter, where P01 works in triode region to act as a resistor. The same analysis can be applied to P02 and C2, but the values of capacitances of C1 and C2 are much different. Therefore, the responses of these two low-pass filters to the same amplitude shift across the receiver coil are much different. The succeeding comparator senses the difference and generates the demodulated command bits. The ratio of P1 to P3 is set to be larger than 1 to provide hysteresis, so is the ratio of P2 to P4. The simulation results are shown in Fig. 31.

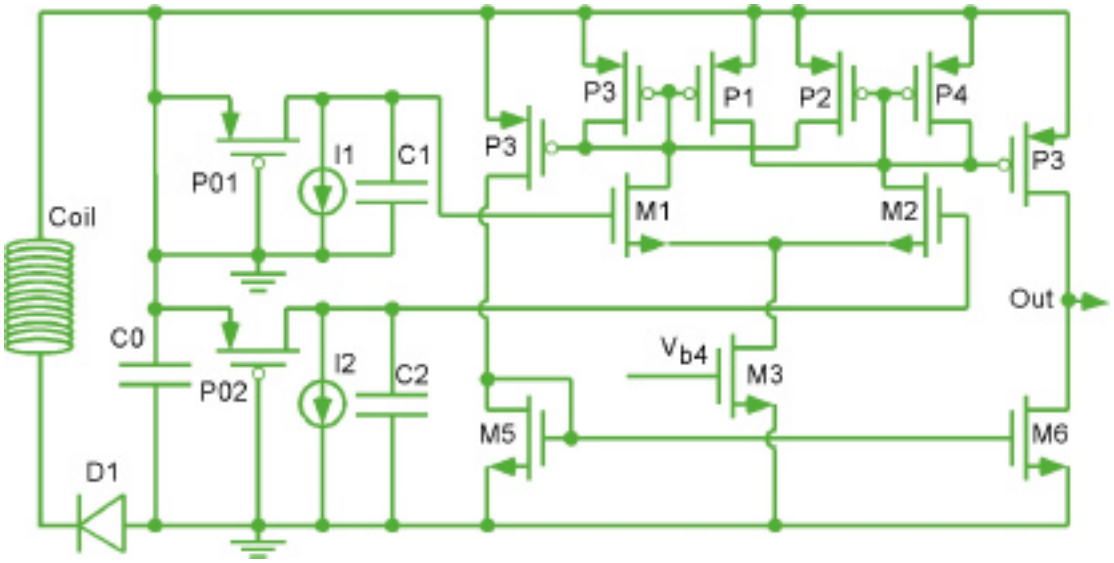

Fig. 30: The schematic of ASK demodulator.

Power-on-Reset circuitry

The Power-On-Reset (POR) circuitry is very simple and is shown in Fig. 32. Current source I1 needs some time to charge capacitor C1 before the buffer input goes to zero. Then POR can keep high for a period of time after power on. The advantage of this circuitry is that no power is consumed after C1 is completely charged.

The simulation result for this circuitry is shown in Fig. 33. It can be seen that a POR pulse of more than 100μs is obtained.

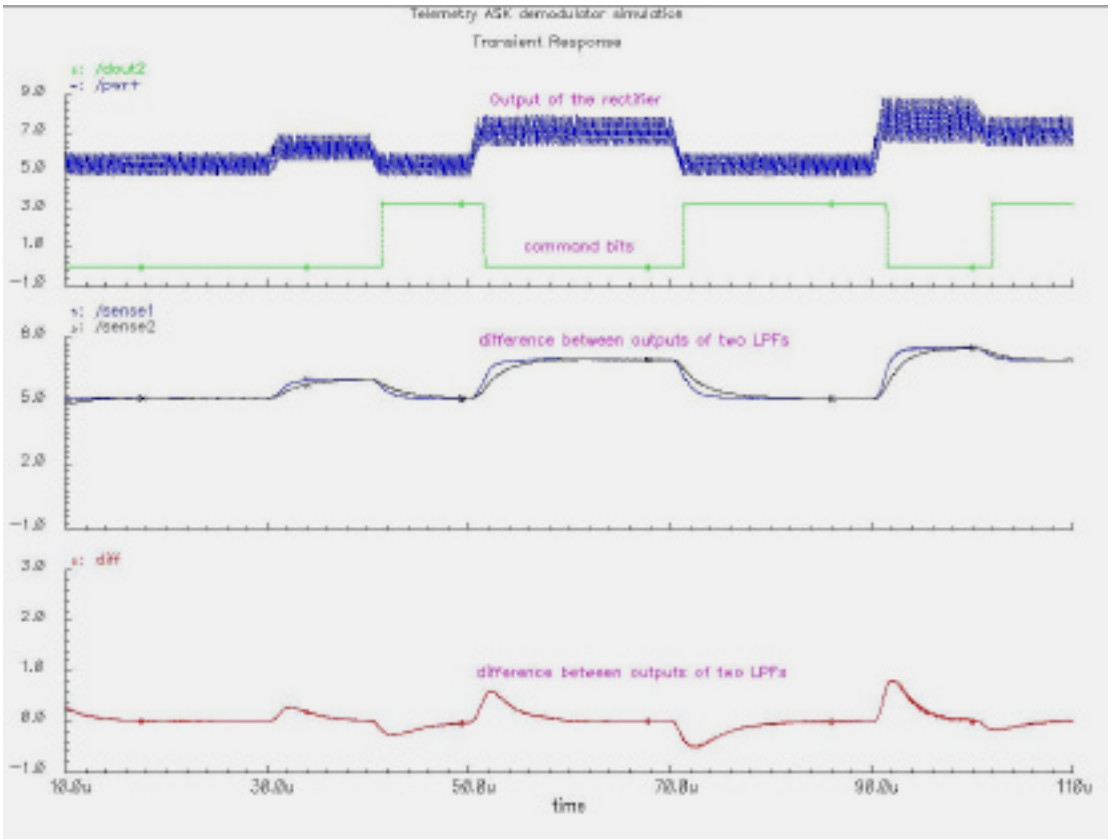

Fig. 31: The simulation results for the ASK demodulator

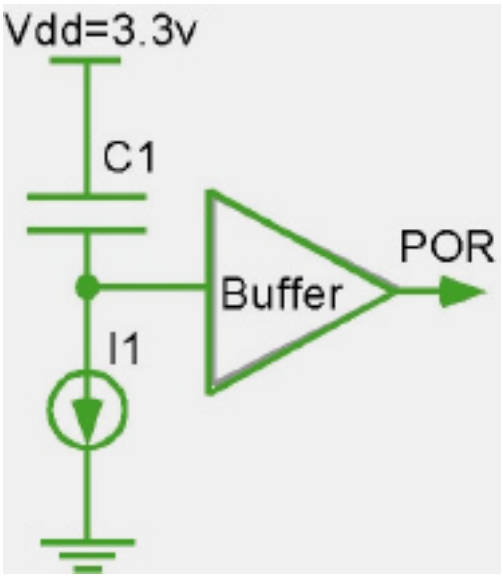

Fig. 32: The Power-On-reset (POR) circuitry.

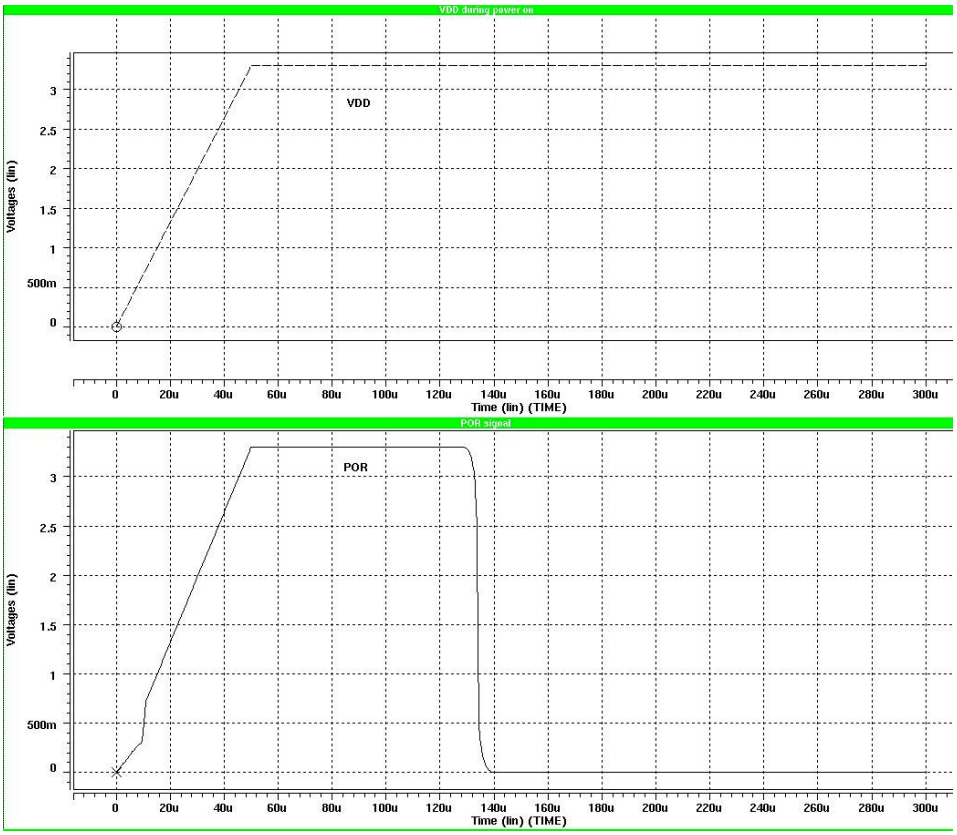

Fig. 33: Simulation results for the POR circuitry.

The Voltage Limiter

The induced voltage across the receiver coil may exceed 15V in some circumstances. This may cause breakdown of the implanted electronic devices. A voltage limiter has been designed, shown in Fig. 34, and will be used to prevent very high induced voltage. When the induced voltage exceeds a specific value, which is dependent on the design as well as the circuit parameters, the limiter begins to sink a large amount of current which will load the receiver coil so that the induced voltage will not rise too high.

Based on Fig. 34, if the induced voltage rises gradually, ND1, ND2, ND3 and P1 begin to conduct more and more current, then P2 begins to conduct, consequently Vgs of N1 becomes large enough that N1 and N2 begin to conduct a large current.

The simulation results for this circuit are shown in Fig. 35, where the circuit is simulated for different fabrication runs given by MOSIS, e.g. FNFP means Fast NMOS and Fast PMOS corners.

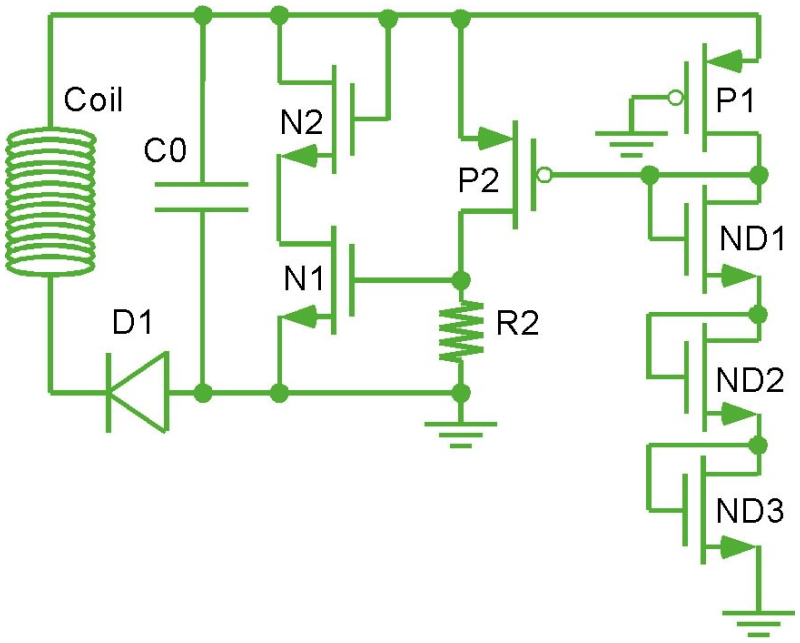

Fig. 34: Circuit diagram of the voltage limiter.

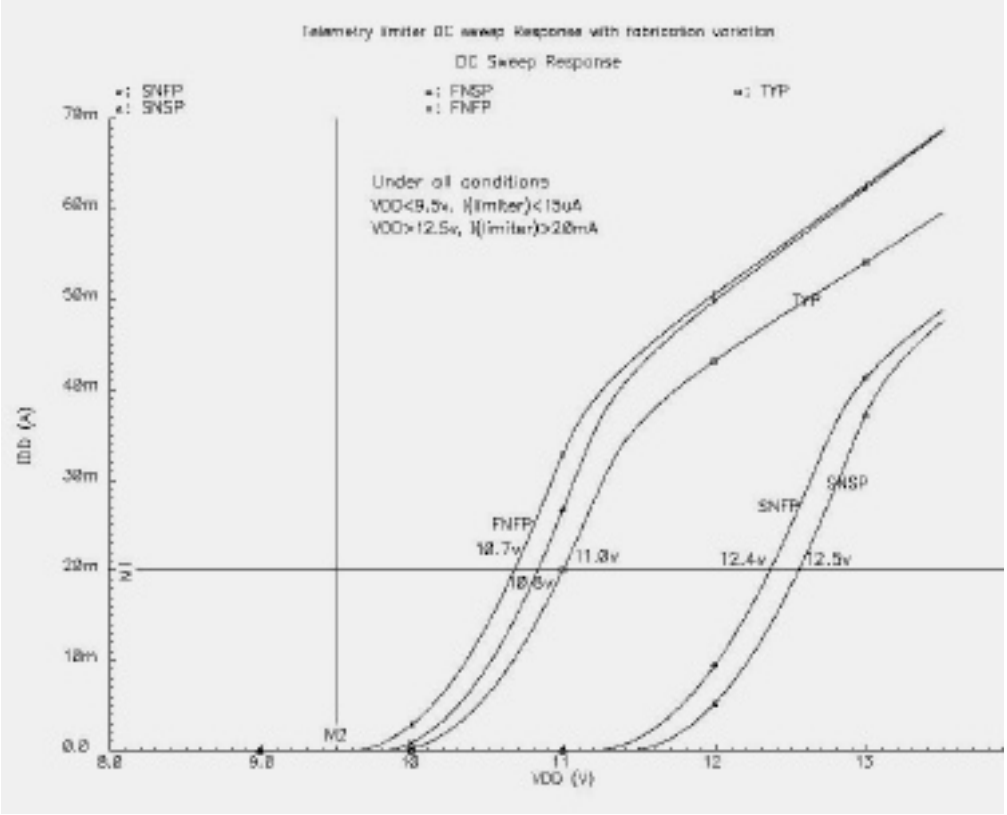

Fig. 35: The simulation results for the voltage limiter circuit.

Overall Front-End Circuitry Power Consumption

The power consumption of the front-end circuitry is listed in Table 3. This total power consumption is significantly lower than previous designs.

Table 3. The power consumption of the front-end circuitry

Circuit Block	Power Consumption
Two Regulators Vout=3.3V. One for Digital circuits, One for Analog circuits	2 x 70µW
A Regulator V=1.65V Used in DSM and the preamplifier	15µW
Clock Recovery	50µW
POR + Voltage limiter	< 3µW after startup and normal condition
Ask Demodulator	20µW
Voltage limiter	<8µW under normal conditions
Total Front-end Circuitry	240µW

6.4. Design of the Manchester Decoder

In Manchester encoding, the actual binary data to be transmitted are not sent as a sequence of logic 1's and 0's. In fact, a logic 1 is indicated by a 0 to 1 transition at the center of the bit and a logic 0 is indicated by a 1 to 0 transition at the center of the bit. Figure 36 shows a typical Manchester encoded signal with the corresponding binary representation of the data (0,0,1,0,1,1) being sent.

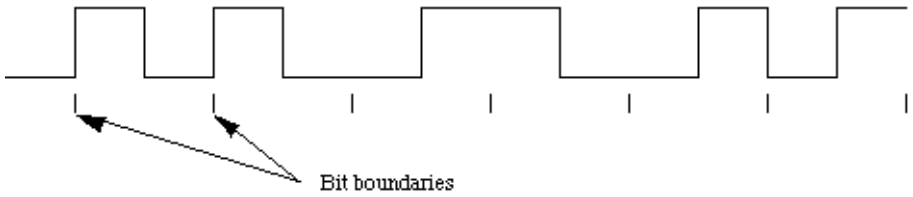

Fig. 36: The waveform for a Manchester encoded bit stream carrying the sequence of bits 001011.

Note that signal transitions do not always occur at the 'bit boundaries' (the division between one bit and another), but that there is always a transition at the center of each bit. Consequently, a Manchester-encoded signal contains frequent level transitions, which allow the receiver to extract the clock, correctly decoding the value and timing of each bit.

Verilog was used to describe the behavior of the Manchester encoder and decoder and verify the logic. The result is shown in Fig. 37. In this diagram, *clk_en* is the original clock used by the encoder, and *clk_out* is the recovered clock from the decoder.

The bit string being sent is *d_en*, and the decoded bit string is *d_out*. It is obvious that the timing information and codes being sent are all extracted correctly.

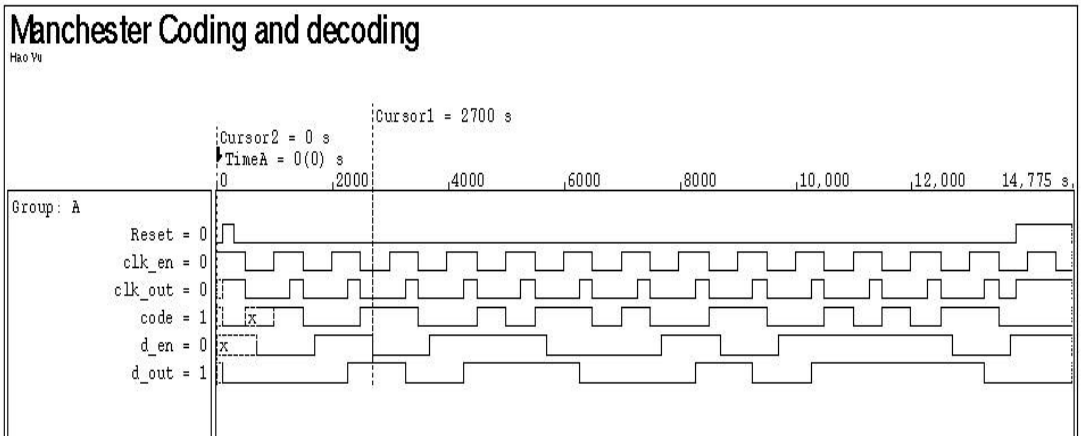

Fig. 37: Simulation results for the Manchester encoder and decoder

During the coming quarter, we plan on submitting the design of the first complete wireless system for recording applications to MOSIS for fabrication. We hope that by the end of the summer we will have this chip back and will be able to test its functionality and performance.

6. Conclusions

We have continued to explore ways to increase the single-unit recording lifetime of chronically-implanted probes. During the past quarter we have continued to follow an 8-shank probe implanted in guinea pig cortex with a large site at the tip (1000μm^2) and a smaller site in the center of the shank 25μm above it (177μm^2). These sites are still recording neural activity after 165 days and will be tracked until they are no longer viable. We are also continuing to explore biopolymer coatings for the probes to modify the tissue reaction to them. These materials can attract neural growth to the probe surface or can reduce adsorption of proteins there. We have deposited polypyrrole and polyethylene glycol on different probes and implanted them in guinea pig cortex. No adverse reaction to these biopolymers is seen three weeks post-implantation histologically nor do the coatings seem to affect the quality of the recordings obtained. More implants with these coatings will be implanted for longer periods of time to further study the tissue reaction to them.

Working with Foster-Miller, Inc., of Waltham, MA, we have developed liquid-crystal polymer-based ribbon cables for the chronic implantation of the probes. The capbles are 25μm and 50μm thick and from 2cm to 9cm in length. The leads are gold and nickel over copper with a 150μm pitch. We are beginning to explore the flexibility

and use of theseprobes in-vivo but the addition of an upper layer of LCP for encapsulation is needed. The cables join with a surface-mount Omnetics NANO connector, with connections made to a silicon ribbon cable using standard ultrasonic wire bonding.

In order to use the front-end-selected 64-site 8-channel probe PIA-2B in-vivo, we have developed a Labview-based user interface for it that allows the user to select recording or test modes and any of the possible site configurations. This probe is now in use in Gyorgy Buzsaki's laboratory at Rutgers and experiments with it here at the University of Michigan are planned for the coming quarter.

In order to successfully fabricate the multiplexed probe, PIA-2, and its 3D counterpart, PIA-3, we have designed and simulated a series of amplifiers for potential use on the probes. These amplifiers offer a gain of 100, bandwidth from 10Hz to 10kHz, power dissipation of 150µW, input-referred noise of 6µVrms/rt.Hz, and a layout area of about 0.084mm^2. They are capacitively coupled to the electrode and differ in the techniques used for input dc bias stabilization. One design uses diodes at the input and output nodes of the feedback capacitor to set the bandwidth and dc bias. A second uses a diode clamp only at the input node, and a third uses a periodically-active clamp transistor pair there. A final configuration uses subthreshold (always on) transistor clamps at input and output nodes to quench the battery and optical currents. The first version is being used for the implementation of PIA-2/-3 as well as with a probe designed for wireless operation with platform-mounted telemetry.

Finally, work has gone forward with the development of telemetry circuits for use with active probes. The latest circuits obtained from a MOSIS fabrication run have been evaluated and work as intended. The voltage regulator produces an output voltage of 5V with a variation of less than 2mV over an input voltage range of 8V to 13V. The variation with load is about 4mV/mA. This is excellent performance. The ripple rejection is 46dB at 4MHz. The regulator consumes 80µA. A Delta-Sigma Modulator has also been developed for the telemetry circuits with an overall power dissipation of 200µW.

In order to reduce the power consumption of the front-end circuitry so that it can function correctly even with very limited received power, some of the circuit blocks have been redesigned and the on-chip power supply voltage has been decreased from 5V to 3.3V. The voltage regulator has been modified for this reduced supply voltage and a new operational amplifier has been designed for lower voltage and increased power-supply rejection. The bandgap reference was also redesigned for the lower supply voltage as were the clock-recovery circuit, the amplitude-shift-keyed demodulator, and the voltage limiter. The redesigned front-end circuitry has a total power dissipation of 240µW at 3.3V. A Manchester decoder for neural signal transmission was also developed. A complete telemetry interface for the active probes will be submitted for MOSIS fabrication this summer with the goal of operating a probe wirelessly by fall.